RECEIVED
CENTRAL FAX CENTER
AUG 2 8 2006

Response Under 37 C.F.R.§1.116
Expedited Procedure
Examining Group 2814

REMARKS

Response to the §102 Rejection of Claims 13-18 and 20

In the June 27, 2006 Office Action, the Examiner finalized previous rejections of claims 13-18 and 20 under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent No. 5,963,800 to Augusto (hereinafter "Augusto") or U.S. Patent No. 6,787,402 to Yu (hereinafter "Yu").

Applicants respectfully traverse the Examiner's §102(b) rejections, on the basis that neither Augusto nor Yu teaches each and every element recited by independent claim 13, from which claims 14-18 and 20 depend.

Claim 13 positively recites a double-gated/double-channel FIN metal oxide semiconductor field effect transistor (MOSFET) having: (1) a bottom Si-containing layer; (2) an insulating region present atop said bottom Si-containing layer, said insulating region having at least one partial opening therein; (3) a gate region in said partial opening, said gate region comprising two regions of gate conductor that are separated from vertical fin-shaped silicon-containing channel regions by an insulating film, said insulating film comprising a gate dielectric and having opposite vertical surfaces adjacent to the vertical fin-shaped silicon-containing channel regions; (4) source/drain diffusion regions abutting said gate region, said source/drain diffusion regions having junctions that are self-aligned to the vertical fin-shaped silicon-containing channel regions and the gate region; and (5) insulating spacers in said partial opening that separate the gate region and the source/drain diffusion regions formed orthogonal to said insulating film, wherein said gate region is between said insulating spacers, and wherein the gate region is self-aligned to the source/drain diffusion regions and the vertical fin-shaped silicon-containing channel regions.

In the June 27, 2006 Office Action, the Examiner alleged that the phrase "double-gated/double channel FIN metal oxide semiconductor field effect transistor (MOSFET)" as recited by claim 13

of the present application has not been given patentable weight because this limitation is recited in the preamble, instead of the claim body, of claim 13.

However, it has been well established that when the preamble is "necessary to give life, meaning and vitality to the claims or counts" and states a necessary and defining aspect of the invention, the preamble is considered as a limitation on the scope of the claim. See Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478 (CCPA 1951). In On Demand Machine Corp. v. Ingram Industries Inc., 78 USPQ2d 1428 (CAFC 2006), the Court of Appeals for the Federal Circuit held that the phrase "high speed manufacture" in the claim preamble necessarily limits the claim, because the preamble states the framework of the invention and serves to focus the reader on the invention that is being claimed.

In the present case, the phrase "double-gated/double channel FIN metal oxide semiconductor field effect transistor (MOSFET)" in the preamble of claim 13 states a necessary and defining aspect of the present invention and is necessary to give life, meaning and vitality to claim 13, by stating the framework of the invention, i.e., double-gated/double channel FET MOSFET, and serving to focus the reader on the invention that is being claim. Therefore, the phrase "double-gated/double channel FIN metal oxide semiconductor field effect transistor (MOSFET)" in the preamble of claim 13 necessarily limits claim 13 and its dependent claims 14-18 and 20, despite the Examiner's allegation.

More importantly, the body portion of claim 13 positively recites a gate region that comprises two regions of gate conductor that are separated from vertical fin-shaped silicon-containing channel regions by an insulating film, said insulating film comprising a gate dielectric and having opposite vertical surfaces adjacent to the vertical fin-shaped silicon-containing channel regions. Such a gate region with two regions of gate conductor, such vertical fin-shaped silicon-containing channel regions, and such an insulating film with opposite vertical surfaces adjacent to the vertical fin-shaped silicon-containing channel regions, as positively recited by the body portion of claim 13, further define the double-gated/double channel FIN MOSFET as recited by the preamble of claim 13. It is thus clear that the body portion of claim 13 following the

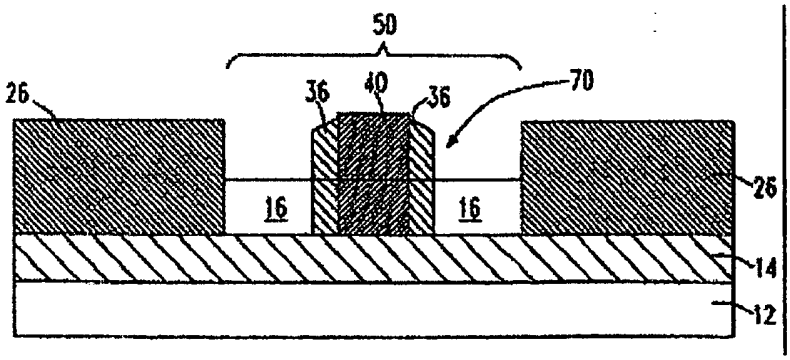
preamble is not a self-contained description of the claim structure; instead, the body portion of claim 13 depends upon the introduction by the preamble of claim 13 of a double-gated/double channel FIN MOSFET for completeness.

Therefore, the phrase "double-gated/double channel FIN metal oxide semiconductor field effect transistor (MOSFET)" in the preamble of claim 13 should be considered a limitation on claim 13 and be given patentable weight.

In the June 27, 2006 Final Office Action, the Examiner referred to various structural elements disclosed in Augusto and Yu in support of the §102(b) rejection of claims 13-18 and 20, by alleging that such structural elements read on the claimed elements positively recited by claims 13-18 and 20 of the present application. However, some of the Examiner's allegations clearly contradict with the actual disclosure of Augusto and Yu and cannot be used to support the §102 rejections of claims 13-18 and 20, as explained in detail hereinafter:

(A). Insulator Region with Partial Opening Therein

Claim 13, from which claims 14-18 and 20 depend, positively recites "an insulating region present atop said bottom Si-containing layer, said insulating region having at least one partial opening therein." Specifically, FIG. 11A and page 12, lines 5-9 of the instant specification describe an insulating region (14+26) present atop a bottom Si-containing layer (12), while the insulating region (14+26) having at least one partial opening (50) therein that extends partially through an upper portion (14) of the insulating region (14+26), as shown below:



At page 3, lines 11-13 of the June 27, 2006 Office Action, the Examiner asserted that the Augusto reference discloses an insulating region that is present atop a bottom Si-containing layer and has at least one partial opening therein, referring to layer 5 or 7 in Fig. 3, column 11, lines 29-46, and Flow 4 of Augusto.

However, Fig. 3 of Augusto clearly labels layer 5 or 7 as "PMOS Source," and column 11, lines 29-46 of Augusto discloses that layer 5 in Fig. 3 is the source of the PMOS transistor. August discloses expressly at column 10, lines 25-26 that layer 5 is an undoped or lowly doped $Si_{1-x}Ge_x$ layer and that layer 7 is a very highly doped p++ graded SiGe layer. Therefore, it is clear that layer 5 or 7 in Fig. 3 of Augusto is composed of semiconductor materials (i.e., $Si_{1-x}Ge_x$ or SiGe) and is **not an insulating region**, despite the Examiner's assertion at page 3, line 11 of the June 27, 2006 Office Action. Further, layer 5 or 7 in Fig. 3 of Augusto is a continuous layer having **no partial opening therein**, despite the Examiner's assertion at page 3, lines 12-13 of the June 27, 2006 Office Action.

The Examiner further asserted on pages 6-7 of the June 27, 2006 that Flow 4, FIGS. 10.1-10.3, and column 14, lines 50-63 of Augusto disclose a SOI structure wherein "an insulating layer is present over the silicon (containing) layer and lists at least 8 materials that are suitable as insulating materials" and that FIG. 7.1 of Augusto shows at least one partial opening.

The disclosure by Augusto at Flow 4, FIGS. 10.1-10.3, column 14, lines 50-63 relates to drain barriers that are made of an insulator that are located between NMOS and PMOS structures. FIG. 7.1 of Augusto shows two openings, each of which extends through a barrier layer that is located between the NMOS and the PMOS.

However, it is clear from FIG. 7.1 of Augusto that the openings in FIG. 7.1 are **not partial openings**, as positively recited by claim 13 and its associated dependent claims of the present invention; instead, the openings in FIG. 7.1 of Augusto extend completely through the barrier layer and are therefore complete openings.

Therefore, nothing in Augusto teaches or suggests "an insulating region present atop said bottom Si-containing layer, said insulating region having at least one partial opening therein," as positively recited by claim 13 and its associated dependent claims 14-18 and 20 of the present application.

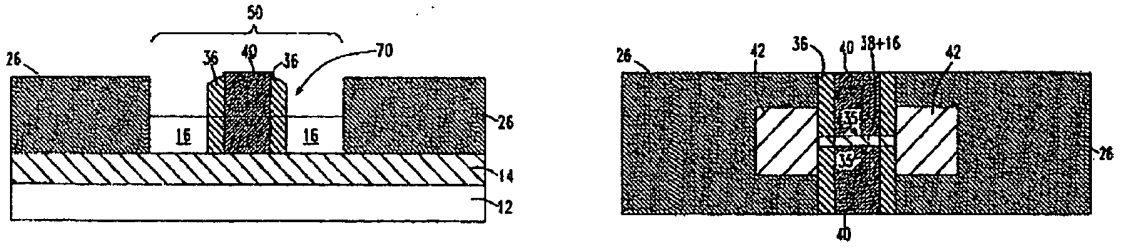
In the June 27, 2006 Office Action, the Examiner alleged that Yu discloses in FIGS. 1 and 4 and column 3, lines 25-35 and 38-40 an insulating region 14 present atop a bottom Si-containing layer 12 having at least one partial opening therein (see Office Action, page 3, lines 11-14). Specifically, the Examiner asserted that Yu discloses at column 3, lines 26-28 "a vertical channel (i.e., at least one partial opening therein) in insulator 14 is created by etching which is similar if not identical to Applicant's partial opening" (see Office Action, page 9, lines 9-11).

However, the insulator layer 14 disclosed by Yu in FIGS. 1 and 4 is a continuous layer having **no partial opening therein**. The disclosure by Yu at column 3, lines 25-35 relates to formation of a vertical channel in FIG. 2 by etching of the silicon layer 16 and the insulator layer 18, but **not the insulator 14**. The disclosure by Yu at column 3, lines 38-40 relates to creation of a "buried-stack," which is the silicon-insulator stack 22 that comprises the etched silicon layer 16 and the etched insulator layer 18 and is buried in a thick layer of gate material 26, as shown in FIG. 4. Therefore, nothing in column 3, lines 25-35 and 38-40 of Yu or other parts of Yu teaches or even suggests that the insulator layer 14 was etched in any manner, much less formation of a partial opening in the insulator layer 14. The Examiner's assertion regarding Yu is not supported by the actual disclosure of Yu and cannot be used to support the rejection of claim 13 and its associated dependent claims 14-18 and 20.

In summary, neither Augusto nor Yu teaches or suggests "an insulating region present atop said bottom Si-containing layer, said insulating region having at least one partial opening therein," as positively recited by claim 13 and its associated dependent claims 14-18 and 20 of the present application.

(B). Insulating Spacers

Claim 13 further recites "insulating spacers in said partial opening [in the insulator region] that separate the gate region and the source/drain diffusion regions." Specifically, FIGS. 11A-11B of the instant specification show insulating spacers (36) located in the partial opening (50) in the insulator region (14+26) that separate the gate region (40) and the source/drain diffusion regions (42), as shown below:



In the June 27, 2006 Office Action, the Examiner asserted that Augusto discloses in FIG. 3 insulating spacers (see Office Action, page 4, lines 3-5).

However, the insulating spacers as shown in FIG. 3 of Augusto are located in an opening that extends through the NMOS source layer 5' or 7', the NMOS channel layer 3', and partially through the NMOS drain layer 1', which are all semiconductor layers instead of insulator layers. Therefore, the insulating spacers as shown in FIG. 3 of Augusto are **not** "insulating spacers in said partial opening [in the insulator region]," as positively recited by claim 13 and its associated dependent claims 14-18 and 20 of the present application.

Further, the insulator spacers as shown in FIG. 3 of Augusto do not separate the gate region 13 and the source/drain diffusion regions 5' or 7', 1', 1, and 5 or 7; instead, the insulator spacers as shown in FIG. 3 of Augusto separates the drain contact 21 from the NMOS source layer 5' or 7' and the NMOS channel layer 3'. Therefore, the insulator spacers as shown in FIG. 3 of Augusto are **not** "insulating spacers... that separate the gate region and the source/drain diffusion regions," as positively recited by claim 13 and its associated dependent claims 14-18 and 20 of the present application.

In the June 27, 2006 Office Action, the Examiner asserted that Yu discloses in FIGS. 3-6 insulating spacers (see Office Action, page 4, lines 3-6).

However, Yu only discloses gate oxide 24 on the sidewalls of vertical segment of silicon layer 16 (see Yu, FIGS. 3-6 and column 3, lines 36-39). First, the gate oxide 24 is not an insulating spacer. Second, the gate oxide 24 is not located in a partial opening in an insulating region. Third, the gate oxide 24 only separates the gates 26a and 26b from the channel 16, but it does not separate the gates 26a and 26b from the source/drain diffusion regions 32 and 34 (see FIGS. 5 and 6 of Augusto). Therefore, nothing in Yu teaches or even suggests formation of insulating spacers, much less insulating spacers that are located in a partial opening in an insulating region and separate a gate region and source/drain diffusion regions.

In summary, neither Augusto nor Yu provides any derivative basis for "insulating spacers in a partial opening [in an insulating region] that separate the gate region and the source/drain diffusion regions," as positively recited by claim 13 and its associated dependent claims 14-18 and 20 of the present application.

Correspondingly, claim 13 and its associated dependent claims 14-18 and 20 patentably distinguish over the Augusto and Yu references, by positively reciting "an insulating region present atop said bottom Si-containing layer, said insulating region having at least one partial opening therein" and "insulating spacers in a partial opening [in an insulating region] that separate the gate region and the source/drain diffusion regions."

Response to the §103 Rejection of Claim 19

In the June 27, 2006 Office Action, the Examiner further rejected claim 19 under 35 U.S.C. §103(a) as being obvious over Augusto as applied to claims 13-18 and 20, further in view of U.S. Patent No. 5,315,144 to Cherne (hereinafter "Cherne") or U.S. Patent No. 6,656,824 to Hanafi et al. (hereinafter "Hanafi").

Claim 19 depends directly from claim 13 and therefore incorporates all the limitations of claim 13.

As mentioned hereinabove, Augusto fails to teach each and every limitation of claim 13, particularly the insulator region with at least one partial opening therein and the insulating spacers located in the partial opening that separates the gate region and the source/drain diffusion region.

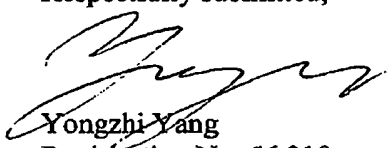
The applied disclosure by Cherne and Hanafi relates only to silicide layers formed atop the source/drain diffusion regions. Therefore, the applied disclosure by Cherne and Hanafi does not remedy such deficiencies of Augusto.

Correspondingly, claim 19 patentably distinguishes over Augusto, Cherne and Hanafi.

CONCLUSION

Based on the foregoing, claims 13-20 as amended herein are in condition for allowance. Issuance of a Notice of Allowance for the application is therefore requested.

Respectfully submitted,



Yongzhi Yang
Registration No. 56,310

SCULLY, SCOTT, MURPHY & PRESSER, P.C.
400 Garden City Plaza, Suite 300
Garden City, New York 11530
(516) 742-4343 (telephone)
(516) 742-4366 (facsimile)
MY:vh